In the outstanding Office Action, the drawings were objected to under 37 C.F.R. § 1.84(p)(4) with regard to reference characters "36" and "42." Further, Claims 5, 9, and 13 were rejected under 35 U.S.C. § 112, first paragraph, with regard to the claimed thickness of the first and second insulating films. Finally, Claims 1, 2, 6, 8, 10, and 12 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,019,527 to Ohshima et al. (hereinafter "the '527 patent"); and Claims 3-5, 7, 9, 11, and 13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the '527 patent in view of U.S. Patent No. 5,482,894 to Havemann (hereinafter "the '894 patent").

In response to the objection to the drawings, submitted herewith is a separate letter requesting approval for drawing changes as well as a clean copy of the amended drawings. Figure 7B has been amended to properly identify element 42.

Applicants respectfully submit that the rejection of Claims 5, 9, and 13 under 35 U.S.C. § 112, first paragraph, is rendered moot by the amendment to those claims. Claims 5, 9, and 13 have been amended to specify that the thickness of the first insulating film is between 100Å and 200Å, and that the thickness of the second insulating film is between 200Å and 400Å. As noted in the Office Action, there is adequate support for these limitations in the specification.

Amended Claim 1 is directed to a semiconductor memory device comprising, *inter alia*, (1) a semiconductor body of a first conductivity type; (2) a stack gate formed on the semiconductor body; (3) a contact material buried to be adjacent to the first side surface of the stack gate; (4) a first insulating film formed on the second side surface and on the upper surface of the stack gate; and (5) a second insulating film formed on the first side surface adjacent to the contact material, the second insulating film covering the entirety of the first insulating film. Claim 1 has been amended to clarify that the second insulating film is

formed on the first side surface adjacent to the contact material and covers the entirety of the first insulating film. The amendment to Claim 1 is supported by the originally filed specification and does not add new matter.

The '527 patent is directed to a method of manufacturing a semiconductor memory, as shown, e.g., in Figures 8A-8I. Referring to those figures, the Office Action indicates that the '527 patent discloses a first insulating film 12 and a second insulating film 11. However, the '527 patent fails to show a second insulating film formed on the first side surface adjacent to the contact material, the second insulating film covering the *entirety* of the first insulating film, as recited in amended Claim 1.[2] Accordingly, Applicants respectfully traverse the rejection of Claim 1 (and dependent Claim 2) as being anticipated by the '527 patent.

Amended independent Claims 6 and 10 recite limitations analogous to the limitations recited by amended Claim 1. Accordingly, for the reasons stated above for the patentability of Claim 1, Applicants respectfully traverse the rejection of Claim 6 (and dependent Claim 8) and Claim 10 (and dependent Claim 12) as being anticipated by the '527 patent.

Regarding the rejection of dependent Claims 3-5, 7, 9, 11, and 13 under 35 U.S.C. § 103(a), Applicants submit that the '894 patent fails to cure the deficiencies of the '527 patent with regard to the second insulating film, as discussed above. Accordingly, Applicants respectfully submit that a *prima facie* case of obviousness has not been established and that the rejection of dependent Claims 3-5, 7, 9, 11, and 13 should be withdrawn.

Thus, it is respectfully submitted that independent Claim 1 (and dependent Claims 2-5), independent Claim 6 (and dependent Claims 7-9), and independent Claim 10 (and dependent Claims 11-13) patentably define over the '527 and '894 patents.

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[2]See, e.g., Figure 8G of the '527 patent.

Consequently, in view of the present amendment and in light of the above discussions, the outstanding grounds for rejection are believed to have been overcome. The application as amended herewith is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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Marked-Up Copy
Serial No: 09/925,418
Amendment Filed on:
08/19/02

IN THE CLAIMS

1. (Amended) A non-volatile semiconductor memory device comprising:

a semiconductor body of a first conductivity type;

first and second semiconductor regions of a second conductivity type, formed apart from each other on the semiconductor body;

a stacked gate formed on the semiconductor body between the first and second semiconductor regions, with a gate insulating film inserted therebetween, the stacked gate having a first side surface, a second side surface opposed to the first side surface, and an upper surface;

an interlayer insulating film formed above the semiconductor body;

a contact material buried to be adjacent to the first side surface of the stacked gate[,] in the interlayer insulating film, the contact material contacting the first semiconductor region;

a first insulating film formed on the second side surface and on the upper surface, [except] but not on the first side surface of the stacked gate adjacent to the contact material; and

a second insulating film formed on the first side surface adjacent to the contact material, [and] the second insulating film covering the entirety of the first insulating film.

5. (Amended) The device according to claim 1, wherein the first insulating film is an oxide-based insulating film having a film thickness of 100Å to 200Å [or less], and the second insulating film is a nitride-based insulating film having a film thickness of 200Å to 400Å [or less].

6. (Amended) A non-volatile semiconductor memory device comprising:

a semiconductor body of a first conductivity type;

first and second semiconductor regions of a second conductivity type, formed apart from each other on the semiconductor body;

a stacked gate formed on the semiconductor body between the first and second semiconductor regions, with a gate insulating film inserted therebetween, the stacked gate including a charge storage layer on the gate insulating film, a control gate on the charge storage layer, and a cap insulating film on the control gate, and the stacked gate having a first side surface, a second side surface opposed to the first side surface, and an upper surface, the first and second surfaces each including side surfaces of the charge storage layer, the control gate, and the cap insulating film;

an interlayer insulating film formed above the semiconductor body;

a contact material buried to be adjacent to the first side surface of the stacked gate[,] in the interlayer insulating film, the contact material contacting the first semiconductor region;

a first insulating film formed on [at least a part of] the side surface of the control gate on the first side surface, and on all of the side surface of the charge storage layer on the first side surface; and

a second insulating film formed on the first side surface adjacent to the contact material [to cover], the second insulating film covering the entirety of the first insulating film.

9. (Amended) The device according to claim 6, wherein the first insulating film is an oxide-based insulating film having a film thickness of 100Å to 200Å [or less], and the second insulating film is a nitride-based insulating film having a film thickness of 200Å to 400Å [or less].

10. (Amended) A non-volatile semiconductor memory device comprising:

a semiconductor body of a first conductivity type;

first and second semiconductor regions of a second conductivity type, formed apart from each other on the semiconductor body;

a stacked gate formed on the semiconductor body between the first and second semiconductor regions, with a gate insulating film inserted therebetween, the stacked gate including a charge storage layer on the gate insulating film, a control gate on the charge storage layer, and a cap insulating film on the control gate, and the stacked gate having a first side surface, a second side surface opposed to the first side surface, and an upper surface, the first and second surfaces each including side surfaces of the charge storage layer, the control gate, and the cap insulating film;

an interlayer insulating film formed above the semiconductor body;

a contact material buried to be adjacent to the first side surface of the stacked gate[,] in the interlayer insulating film, the contact material contacting the first semiconductor region;

a first insulating film formed on [at least a part of] the side surface of the control gate on the first side surface, on all of the side surface of the charge storage layer on the first side surface, [at least a part of] on the side surface of the control gate on the second side surface, and on all of the side surface of the charge storage layer on the second side surface; and

a second insulating film formed on the first side surface adjacent to the contact material [to cover], the second insulating film covering the entirety of the first insulating film, the second insulating film being formed on the second side surface [to cover], and covering the entirety of the first insulating film[,] and the upper surface.

13. (Amended) The device according to claim 10, wherein the first insulating film is an oxide-based insulating film having a film thickness of 100Å to 200Å [or less], and the second insulating film is a nitride-based insulating film having a film thickness of 200Å to 400Å [or less].